SIMPLE SWITCHER® PCB Layout Guidelines

National Semiconductor
Application Note 1229
Sanjaya Maniktala
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Introduction

One problem with writing an Application Note on PCB layout is that the people who read it are usually not the ones who are going to use it. Even if the designer has struggled through electromagnetic fields, EMC, EMI, board parasitics, transmission line effects, grounding, etc., he will in all probability then go on with his primary design task, leaving the layout to the CAD/layout person. Unfortunately, especially when it comes to switching regulators, it is not enough to be concerned with just basic routing/connectivity and mechanical issues. **Both the designer and the CAD person need to be aware that the design of a switching power converter is only as good as its layout.** Which probably explains why a great many of customer calls received, concerning switcher applications, are ultimately traced to poor layout practices. Sadly, these could and should have been avoided on the very first prototype board, saving time and money on all sides.

The overall subject of PCB design is an extremely wide one, embracing several test/mechanical/production issues and also in some cases compliance/regulatory issues. There is also a certain amount of physics/electromagnetics involved, if a clearer understanding is sought. But the purpose of this Application Note is to reach the audience most likely to use it. Though there is enough design information for the more experienced designer/CAD person, the Application Note includes a quick-set of clear and concise basic rules that should be scrupulously followed to avoid a majority of problems. In particular, we have provided **recommended starting points for layout when using the popular LM267x, LM259x and LM257x families (Figure 2)** The focus is on the step-down (Buck) Simple Switcher ICs from National, but the same principles hold for any topology and switching power application.

Most of the issues discussed in this Note revolve around simply assuring the desired performance in terms of basic electrical functionality. Though luckily, as the beleaguered switcher designer will be happy to know, in general all the electrical aspects involved are related and point in the same general 'direction'. So for example, an 'ideal' layout, i.e. one which helps the IC function properly, also leads to reduced electromagnetic emissions, and vice-versa. For example, reducing the area of loops with switching currents will help in terms of EMI and performance. However the designer is cautioned that there are some exceptions to this general 'trend'. One which is brought out in some detail here is the practice of 'copper-filling', which may help reduce parasitic inductances and reduce noise-induced IC problems, but can also increase EMI.

Quick-Set of Rules for SIMPLE SWITCHER PCB Layout (Buck)

a) Place the catch diode and input capacitor as shown in *Figure 2*.

b) For high-speed devices (e.g. LM267x) do not omit placing input decoupling/bypass ceramic capacitor (0.1 µF–0.47 µF) as in *Figure 2*.

c) Connect vias to a Ground plane if available (optional, marked 'X' in *Figure 2*)

d) If vias fall under tab of SMT power device, these are considered 'thermal vias'. Use correct dimensions as discussed to avoid production issues. Or place the vias close to but not directly under the tab.

e) Route feedback trace correctly as discussed, away from noise sources such as the inductor and the diode.

f) Do not increase width of copper on switching node injudiciously.

g) If very large heatsink area is required for catch diode (having estimated the heatsink requirement correctly) use isolation as discussed.

h) For higher power SMT applications, use 2 oz board for better thermal management with less copper area.

Introduction (Continued)

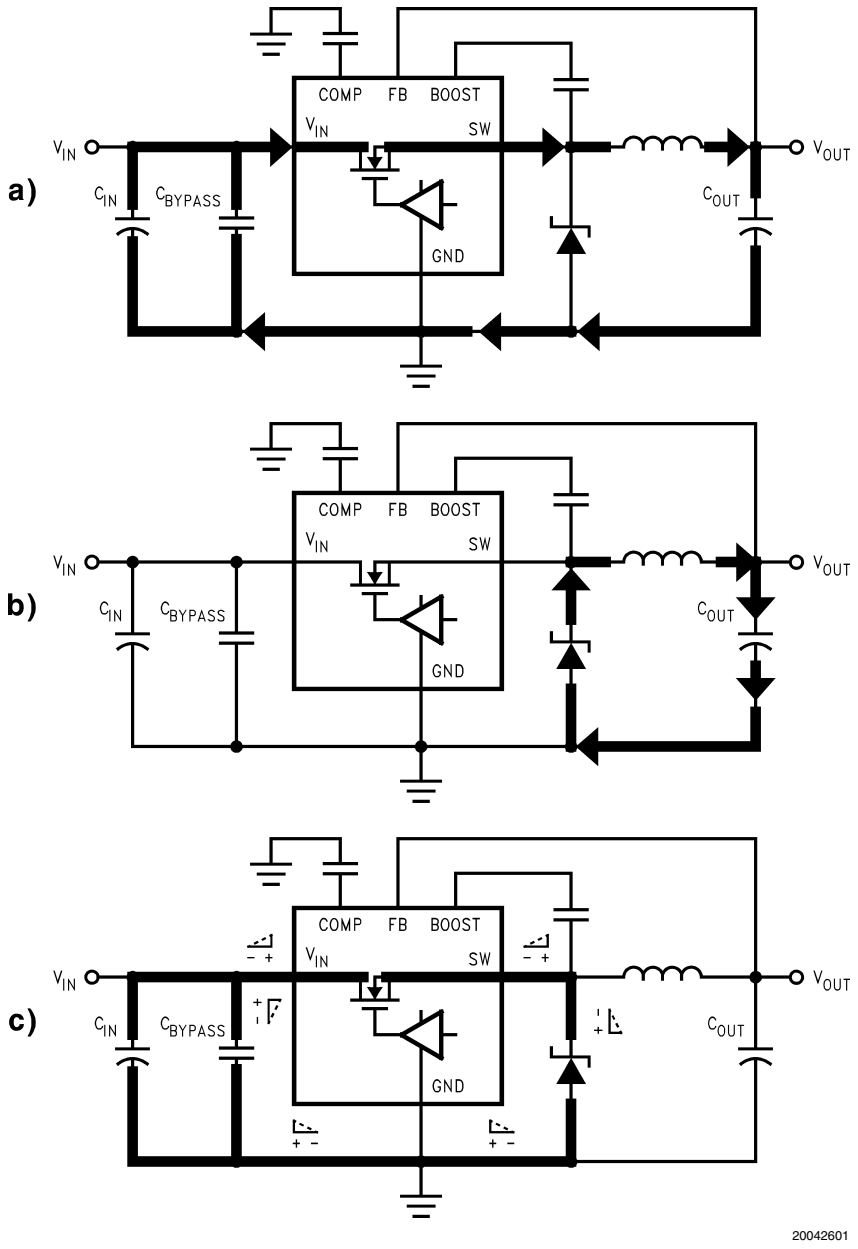

FIGURE 1.

The AC and DC Current Paths

Referring to *Figure 1a*, the bold lines represents the main (power) current flow in the converter during the time the switch is ON. As the switch turns ON, the edge of the of the current waveform is provided largely by CBYPASS, the remainder coming mainly from CIN. Some slower current components come from the input DC power supply (not shown) and also refresh these input caps. *Figure 1b* represents the situation when the switch is OFF. We can therefore see that in certain trace sections, current has to start flowing suddenly during the instant of switch turn-off and in some sections it needs to stop flowing equally suddenly. *Figure 1c* represents the 'difference', i.e. traces shown bold in this Figure are those where the current flow **changes suddenly**.

During the turn-on transition the picture reverses, but the 'difference' trace sections are the same. Therefore during either switch transition, 'step changes' of current take place in these difference sections. These traces encounter the harmonic-rich rising or trailing edges of the current pedestal waveform. The difference traces are considered 'critical' and deserve utmost attention during PCB layout. It is often stated colloquially, that 'AC current' flows in these trace sections, and 'DC current' in the others. The reason is that the basic switching PWM frequency forms only a fraction of the total harmonic (Fourier) content of the current waveform in the 'AC' traces. In comparison, where 'DC current' flows, the current does not change in a stepped fashion and so the harmonic content is lower. It is also no surprise that the DC

The AC and DC Current Paths

(Continued)

sections are those in series with the main inductor, because it is known that inductors have the property of preventing sudden changes in current (this is analogous to a capacitor which 'resists' sudden changes in voltage).

Summing up: **In switching regulator layout, it is the AC paths that are considered critical, whereas the DC paths are not. That is the only basic rule to be kept in mind, and from which all the others follow. This is also true for any topology.** Perform an analysis of the current flow for any topology in the same manner as we did for the Buck, to find the 'difference traces': and these traces are by defintion the 'critical' ones for layout.

What is the problem with step current changes anyway? In a resistor for example, this causes no unexpected/ unidentifiable problem. The voltage is given by V=IR, and so for a given change of current, the voltage will change proportionally. For example, a **0.5 cm wide Cu trace of thickness 1.4 mil has a resistance of 1milliohm per cm length** (at 20 degC). So it seems that a 1 inch long trace with a current changeover of 1A, would produce a change in voltage of only 2.5 millivolts across the trace, which is insignificant enough to cause the control sections of most ICs to misbehave. But in fact the induced voltage is much larger. The important thing to realize is that traces of copper on a PCB, though barely resistive, are also inductive. Now, the oft-repeated thumb-rule is that **'every inch of trace length has an inductance of about 20 nH'**. Like the trace resistance, that too doesn't seem much at first sight. But it is this rather minute inductance which is in fact responsible for a great many customer calls in SIMPLE SWITCHER applications!

The equation for voltage across an inductance is V=L*dI/dt, and so the voltage does not depend on the current but on the *rate* of change of the current. This fact makes all the difference when the 1A change we spoke about occurs within a very short time. The induced voltage can be very high, even for small inductances and currents, if the dI/dt is high. A high dI/dt event occurs during transition from *Figure 1a* to *Figure 1b* (and back) in all the AC trace sections (shown bold in *Figure 1c*). The induced voltage spike appears across each affected trace, lasting for the duration of the crossover.

To get a better feel for the numbers here: **the change in current in the AC sections of a typical buck converter is about 1.2 times the load current during the switch turn-off transition and is about 0.8 times the load current during the switch turn-on transition** (for an 'optimally' designed Buck inductor, as per inductor design guidelines in the relevant Datasheets/Selection Software). The transition time is about 30 ns for high speed Fet switchers like the LM267x, and is about 75 ns for the slower bipolar switchers like the LM259x series. This also incidentally means that the voltage spikes in the high-speed families can be more than twice that in the slower families, for a comparable layout and load. Therefore **layout becomes all the more critical in high-speed switchers**.

So, one inch of trace switching say 1A of instantaneous current in a transition time of 30 ns gives 0.7V, as compared to 2.5mV (that we estimated on the basis of resistance alone). For 3A, and two inches of trace, the induced voltage 'tries' to be 4V! In *Figure 1c*, the small triangles along the sections indicate the direction of the momentary induced voltage, as the converter changes from the situation in *Figure 1a* to that in *Figure 1b* (switch turn-off). We can see that assuming that the ground pin of the IC is the reference point, the switching node (marked 'SW') tries to go negative (all its series trace sections adding up). Similarly the input pin (marked 'VIN' goes high through series contributions in all its related sections. *Figure 1c* represents the picture during the turn-off transition. During the turn-on transition all the induced voltage polarities shown are simply reversed. In that case, the VIN pin is dragged low, and the switching node pin is dragged high momentarily.

The astute designer will recognize that this was to be expected since any inductance, even if it is parasitic, demands to be 'reset', which means that the volt-seconds during the on-time must equal and be opposite in sign to the volt-seconds during the off-time.The designer will also realize that till these parasitic trace inductances reset, they do not 'allow' the crossover to occur. So for example, traces which were carrying current prior to switch turn-off will 'insist' on carrying current till the voltage spikes force them to do otherwise. Similarly, the traces which need to start carrying current will 'refuse' to do so till the spikes across them force them to do likewise. Since switching losses are proportional to crossover time, even if these voltage spikes do not cause anomalous behavior, they can degrade efficiency. For example, in transformer-based flyback regulators, when the the primary number of turns is much larger than the secondary turns, designers may be surprised to learn how much the secondary side trace inductances alone can degrade efficiency. This is because any **secondary side uncoupled (trace/transformer leakage) inductances reflect into the primary side as an equivalent parasitic inductance in series with the switch. This adds an additional term to the effective leakage as seen by the switch that equals the secondary inductance multiplied by square of the turns ratio** (turns ratio being Np/Ns). Therefore the dissipation in the flyback clamp (zener/RCD) can increase dramatically, lowering efficiency. One lesson here is that though 'leakage inductance' (from traces or the transformer) is considered 'uncoupled', in reality it can make its presence severely felt from one side of the transformer to the other. So it is not totally 'uncoupled' at all! In fact this happens to be the main reason why flybacks with low output voltages (high turns ratio) show poorer efficiency as compared to higher output flybacks. Therefore, reducing critical trace inductances is important for several reasons: efficiency, EMI, besides basic functionality.

The momentary voltage spikes which last for the duration of the transition can be very hard to capture on an oscilloscope. But they may be presumed to be present if the IC is seen to be misbehaving for no 'obvious reason'. These spikes, if present with sufficiently high amplitude, can propagate into the control sections of the IC causing what we call here a controller 'upset'. This leads to the observed performance anomalies, and in rare cases this can even cause device failure. Since none of these spike-related problems can be easily corrected, or band-aided, once the layout is initially bad, the important thing is to get the layout 'right' to start with.

The designer may well ask, why is it that these step current changes are a problem with the parasitic trace inductances, and not with the main inductor of the Buck converter? That is because all inductors try to resist any sudden current change. But since the main inductor has a much larger inductance (and energy storage) as compared to the parasitic trace inductances, it therefore ends up 'dominating'. From V*dt=L*dI we can also see that if L is large, a much higher voltseconds (V*dt) is required to cause a given

The AC and DC Current Paths

(Continued)

change in current. The trace inductances therefore simply 'give in' first before the main inductor does. But they certainly don't go down without a fight...and the voltage spikes bear testimony to this!

Notice that the currents in the signal traces in the schematic are not shown. For example those connected to the compensation node (marked 'COMP') or bootstrap (marked 'BOOST') carry relatively minute currents and therefore are not likely to cause upsets. They are therefore not critical and can be routed relatively 'carelessly'. The feedback trace is an exception, and will be discussed later. The Ground pin of the IC is another potential entry point of noise pickup. Inexperienced designers often grossly under estimate the needs of this pin, particulary for Buck converters. They assume that since the main power flow in a Buck converter does not pass through the ground pin, the 'current through the ground pin is very low', and therefore the trace length leading up to this pin is not critical. In fact, though the average current through this pin is very low, the peak current or its dl/dt is not. Consider the switch driver as shown schematically in *Figure 1*. Clearly it needs to supply current to drive the switch. In any Fet operated as a switch, large peak to peak instantaneous current spikes are needed to charge and discharge the gate capacitance. This is essential so as to cause the Fet to switch fast, and this reduces the switching/crossover losses inside the switch and improves the overall efficiency of the converter. (Actually, in a practical IC, the 'spike' of current comes from the bootstrap capacitor, and then the bootstrap capacitor is quickly refreshed by the internal circuitry of the IC ---- it is the refresh current that passes through the ground pin). Further, as in any high-speed digital IC, parts of the internal circuitry, clocks, gates, comparators etc., can turn on and off suddenly, leading to small but abrupt changes in the current through the ground pin. This can cause 'ground bounce' which in turn can lead to controller upsets. Therefore the length of the trace to the Ground pin also needs to be kept as small as possible. This also implies that **the input capacitors, especially the bypass capacitor 'CBYPASS' should be placed very close to the IC**, even for a Buck IC.

Placing Components 'acap' (as Close as Possible)

One has heard this before: "component X needs to be 'acap' ". Soon we are told the "component Y too needs to be 'acap' ". Then "Z too". And so on. Which would be physically impossible because matter cannot occupy the same place at the same time! So which one comes first? This is the million-dollar predicament always facing switcher layout.

The troubling trace lengths are those indicated *Figure 1c*. To keep them small, clearly two components need to be acap. These are the input bypass capacitor and also the catch diode. Consider the input capacitor section first.

In the schematic there are in two input capacitors shown. These are marked 'CIN' and 'CBYPASS' respectively. The purpose of the total input capacitance is to reduce the voltage variations at the input pin. The variations are mainly due to the pulsed input current waveshape, as demanded by a Buck topology. Note that for this particular topology, the output capacitor current is smooth (because the inductor is in series with it). In a Boost topology the situation is reversed: i.e. the input capacitor current is smooth and the current into the output capacitor is pulsed. This makes the demand for input decoupling less stringent than in a Buck (or Buck-Boost). In a Buck-Boost or 'flyback', both the input and the output capacitor currents are pulsed, and input decoupling is required not only for the control-section/drivers of the IC but for the input current step waveform of the power stage. Designers familiar with a Cuk topology know that in this case both input and output currents are smooth. The Cuk converter is therefore often called the 'ideal DC to DC' converter, and expectedly its parasitic inductances can be largely ignored ---- because there are no AC trace sections in the sense we described.

Now if the input power to a Buck converter was coming through long leads from a distant voltage source, the inductance of the incoming leads would seriously inhibit their ability to provide the fast changing pulsed current shape. So an on-board source of power is required right next to the converter, and this is provided by the input capacitor. It provides the pulsed current, and then is itself refreshed at a slower rate (DC current) from the distant voltage source.

However, since the input capacitor is fairly large in size, it may not be physically possible to place it as close as desired. Especially for very high speed switchers such as the LM267x series (note that a **'high speed' switcher as defined here, is one with a very small crossover/transition time, and it does not necessarily have to be one with a high switching frequency**). In addition, the Equivalent Series Resistance ('esr') and Equivalent Series Inductance ('esl') of the main input capacitor may be too high, and this can cause high frequency input voltage ripple on the VIN pin.

For the Buck converter schematic as shown in *Figure 1*, the input pin connects not only to the Drain of the Fet switch, but also provides a low internally regulated supply rail to the control sections of the IC. But no real series pass regulator can 'hold off' very fast changes in the applied input voltage. Some noise will feed through into the control section and then much will depend on the internal sensitivity of the IC to noise (related to its design, internal layout, process/logic family). It is therefore best to try to keep voltage on the VIN pin fairly clean --—from a high frequency point of view. Note that it is not being suggested here that one responds to this statement by increasing the input capacitance indiscriminately, because we are not talking about the natural input voltage ripple which occurs at the rate of the switching frequency (e.g. 100 kHz–260 kHz). Our concern here is the noise occurring at the moment of the transitions, and this noise spectrum peaks at around 10 MHz–30 MHz, as determined by the transition/crossover time of the switch. The crossover time has nothing to do with the basic PWM switching frequency, but does ofcourse depend on the type of switch used i.e. bipolar or Fet.

Therefore a high frequency 'bypass' or 'decoupling' capacitor with small or no leads, shown as 'CBYPASS' in *Figure 1*, is to be placed very close to the VIN and GND pins of the IC. This is usually a 0.1 µF–0.47 µF (monolithic) multilayer ceramic (typically X7R type, size 1206 or the more recent 'inverted' termination version of this popular size, the '0612' ---- also note that smaller sized ceramic caps generally have higher esr/esl, but check before use). Since now this component provides the main pulsed current waveshape, the bulk capacitor shown as 'CIN', may be moved slightly further up (about an inch) without any deleterious effect. For lighter loads, and if it is possible to place the input bulk capacitor very close to the IC, the high frequency bypass capacitor may sometimes be omitted. **But for high-speed switchers like the LM267x, the input ceramic bypass capacitor is considered almost mandatory for any application.**

Placing Components 'acap' (as Close as Possible) (Continued)

The position of the catch diode is also critical. It too needs to be acap. Now, every topology has a node called the 'switching node'. This is the 'hot' or 'swinging' end of the switch. For integrated switchers, this node can also be an easy entry point for noise feed-through into the control sections. Note that the problem is not caused by the simple fact that the voltage at this node swings, for it is designed for exactly that situation in mind. The problem is with the additional noise spikes riding on top of the basic square voltage waveform, arising from the trace inductances as explained earlier. Therefore, **it is essential to place the catch diode very close to the IC and connect it directly to the SW pin and GND pins of the IC, with traces that are very short and fairly wide** . In some erroneous layouts, where the catch diode was not appropriately placed to start with, the converter could be 'bandaided' by a small series RC snubber. This consists typically of **a resistor (low inductive type preferred) of value 10Ω–100Ω and a capacitor, which should be ceramic of value 470 pF–2.2 nF.** Larger capacitance than this would lead to unacceptably higher dissipation ($=1/2*C*V^2*f$), chiefly in the resistor, and would serve no additional purpose. However, note that this **RC snubber needs to be placed very close to and across the Switching pin and Gnd pin of the IC, with short leads/traces.** Sometimes designers think that this is 'across the diode', because on the schematic there is no way to tell the difference. However, particularly when the diode is a Schottky, the primary purpose of such a snubber is to absorb the voltage spikes of the trace inductances. Therefore its position must be such that it provides bypassing of the critical or AC trace sections of the output side as shown in *Figure 1c* (right hand side of the switcher) ----which means it must be close to the IC. Of course, as mentioned previously, it is best to get the layout right to start with, rather than adding such extra components.

Remaining component placements can be taken up only after the input bypass capacitor and the catch diode are firmly in place and are both acap. The traces to either of these two components should be short, fairy wide, and should not go pass through any vias on the way to the IC. For SMT boards this implies that the input capacitor and catch diode are on the same layer as the IC. **In *Figure 2* suggested PCB starting points are provided for several switchers.** All of them focus on placing these two critical components correctly. These layouts are strongly recommended for most applications. **The 'X' marks suggest the recommended location where vias can be used to connect to a Ground Plane (if present).**The remaining components can be placed relatively carelessly (though in doing so, there may be slight impact, for example on the accuracy of the output voltage rail and its ripple, but nothing compared to what can happen if the input decoupling cap and catch diode are incorrectly placed). Trace routing is now discussed in more detail.

Placing Components 'acap' (as Close as Possible) (Continued)

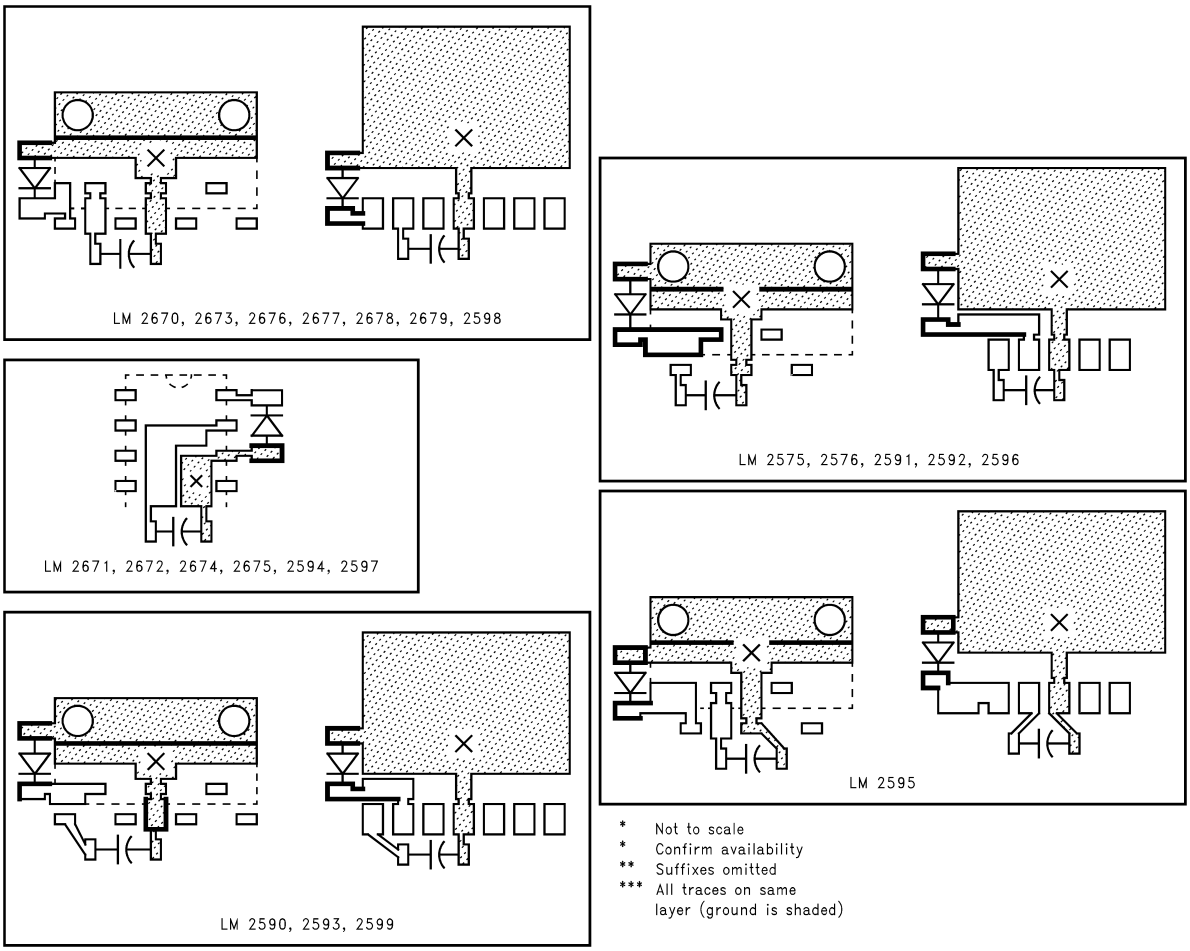

FIGURE 2. Recommended Layout Starting Points

Routing the Traces

As mentioned above, it is not advisable to route any of the critical traces through 'vias'. Vias are considered useful from a purely CAD perspective for 'layer jumping', but are often used indiscriminately as they seem an easy solution to connectivity problems. But they also add impedance, and that is exactly what we are trying to avoid. The inductance of a via is given by

$$L = \frac{h}{5}\left(1 + \ln\frac{4h}{d}\right) nH$$

where 'h' is the height of the via in mm (equal to the thickness of the board, commonly 1.6 mm), and 'd' is the diameter in mm. Therefore a single via of diameter 0.4 mm on a standard 1.6 mm board gives an inductance of 1.2 nH. It may not sound much, but it is almost twice that of a wire of the same length and diameter. **It has been seen empirically that for the high speed LM267x series, if the bypass capacitor is connected through vias to the IC, occasional field problems do arise.**So if vias have to be used for some reason, **several vias in parallel will yield better results than a single via. And larger via diameters would help further (unless they are being used as 'thermal vias'** --- discussed later).

It is also said that "the traces also need to be 'wide' and 'short' ". The necessity of short traces is clearly understood, usually intuitively, by most engineers. In fact the thumbrule of '20 nH per inch' also implies that trace inductance is almost proportional to length. However, **a common 'intuitive' mistake is to assume that inductance is inversely proportional to the width of the trace**. So some engineers mistakenly 'add copper' lavishly to critical traces (though there are some other reasons why this may be being done, and these will be discussed later). A first approximation for the inductance of a conductor having length 'l' and diameter 'd' is

$$L = 2l \bullet \left(\ln\frac{4l}{d} - 0.75\right) nH$$

where l and d are in centimeters. Note that the equation for a PCB trace is not much different from that of a wire.

Routing the Traces (Continued)

$$L = 2l \bullet \left(\ln \frac{2l}{w} - 0.5 + 0.2235 \frac{w}{l}\right) \text{ nH}$$

where 'w' is the width of the trace. For PCB traces, L hardly depends on the thickness of the copper (1 oz or 2 oz board). Both the above equations are plotted in *Figure 3*. It will be seen that for a given length, a PCB trace of width 'x' has higher inductance than a wire of diameter 'x'. In fact **the width of a PCB trace has to be about 1.78 times the diameter of a wire for the same inductance**.

A wire of AWG 20 has a diameter of 32 mils (or 0.081 cm). So for a length of one inch (1000 mils or 2.54 cm) L equals 21 nH (which is the usual thumbrule). We can see that L is almost proportional to length. But if we double the diameter to 0.16 cm, L equals 17 nH, which is not much different from 21 nH. This indicates a non-linear relationship. Referring to *Figure 3*, where the above function is plotted out (dotted lines are for a PCB trace), we can see that **the diameter/width of a wire/trace has to typically increase by a factor of 10 for the inductance to halve**. The relationship of L to d is therefore logarithmic in nature. The reason for this is the effects of mutual inductance between parallel sections/strips of the conductor.

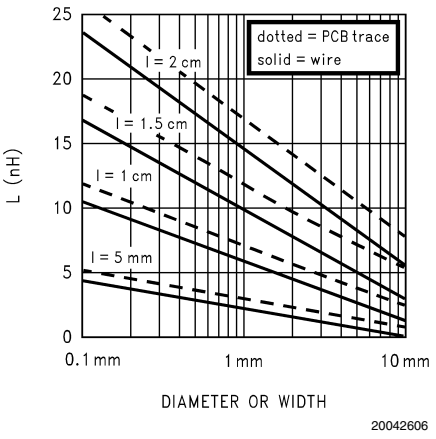

FIGURE 3. Inductance of Wire of Length '1'

'Beefing up' traces to reduce the effects of parasitic inductances should be a last resort. **Decreasing the length of the trace should be the first step. Increasing the width of certain traces can in fact become counterproductive.** In particular, the trace from the switch node to the diode is 'hot' from an EMI point of view. This is not only because of the AC (high frequency) current it carries, but because of its voltage, which is a switched waveform. Any conductor with a varying voltage, irrespective of the current, becomes an antenna if its dimensions are large enough. Radiated emissions from this antenna can cause undesirable common-mode interference in its vicinity. Therefore this calls for the area of the copper around the switching node to be reduced, not increased. Large planes of switched voltage also cause capacitive noise coupling into nearby traces. On a typical SMT board, if the opposite side happens to be a 'ground plane', noise from the switching node can couple through the FR4 dielectric of the PCB into the Ground plane. No Ground plane is 'perfect', and therefore this injected high frequency noise can also cause the ground plane to not only radiate, but to pass noise onto the IC through 'ground bounce'. Some people suggest that a copper island, exactly the same size/shape as the switching-node island be created on the opposite side of the PCB, connected through several vias. This is supposed to prevent 'capacitive cross-talk' to other traces and to enhance thermal dissipation. But this obviously also leads to the breaking-up/partioning of the Ground plane. This defeats the very purpose of Ground plane as it can cause strange effects arising due to the odd current flow patterns in the now divided Ground plane. In general, **the Ground plane should be kept continuous/unbroken as far as possible, or it could behave like a slot antenna. For the switching node therefore, the best option is to keep the amount of copper around it to the actual minimum requirement.**

Some basic physics to be reminded of here: electric fields are caused by electric charge, and magnetic fields by currents. But if an electric field varies with time, it produces a corresponding magnetic field. However magnetic fields are associated with currents. Therefore AC voltages (varying electric fields) on opposite planes of copper on a PCB cause a 'displacement current' (capacitive coupling current) through the FR4 dielectric. Similarly, a varying magnetic field causes an electric field. So for example in a transformer, when we pass AC current (varying magnetic field) in a winding, we get Faraday induced voltages (electric field). Whenever voltage or current is switched, an electromagnetic field is generated, which produces EMI. And this EMI is inadvertently 'helped' by antenna structures. Therefore, on a PCB layout, **the area enclosed by all current loops carrying 'AC (switched) current' must be kept small. Similarly the area of copper planes with 'AC (switched) voltage' must be kept small. Both can behave as antennae. In addition, traces carrying switching currents/voltages must also be kept away from 'quieter' traces to avoid cross-coupling. Further, since 'sharp edges' are known to cause an increase in field strengths, two 45 degree bends in a trace are preferred to a single 90 degree bend.**

Copper Filling: when to Stop

Adding copper lavishly to traces serves some purpose occasionally, sometimes none at all, and sometimes it even works against the design in an unintended manner. There may be no simple hard and fast rules here. Judiciousness needs to be applied. But first it is instructive to consider some of the 'reasons' why copper is lavished, and to the degree it is really required. Most often the requirements are actually much less than predictions based on 'gut instinct':

We will take each of these separately:

A) CURRENT HANDLING CAPABILITY

If we multiply the width of a trace with its thickness we get the 'cross sectional area' of the conductor. This determines the resistance (per unit length) of the conductor and the consequent self-heating. This leads to an estimable temperature rise. It is important to note that the 'current handling capability' is therefore not a 'stake in the ground' as some people think, but is related to a permissible temperature rise.

Copper Filling: when to Stop

(Continued)

Mil Standards call for maximum 20˚C rise, but 30˚C–40˚C are also common. *Figure 4* is a chart which helps in the correct estimation.

Current Density Curve for Outer Layer PCB Copper Etch

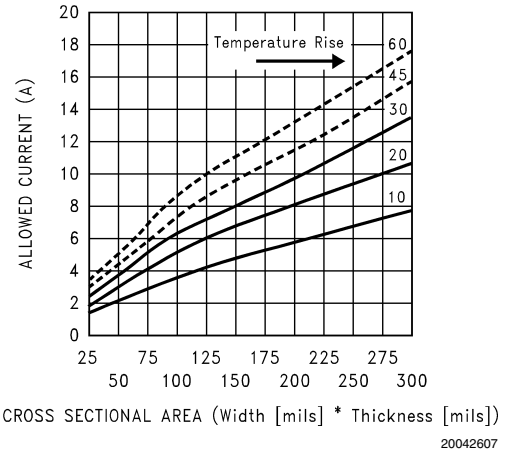

FIGURE 4. MIL-STD-275E Curves for Current Density vs. Temperature Rise

Commercial PCB's are often referred to as '1 oz' or '2 oz' for example. This refers to the weight of copper in ounces per square foot deposited on the copper clad laminate. **1 oz is actually equivalent to 1.4 mils copper thickness (or 35 µm). Similarly 2 oz is twice that**. We are only considering outer layers (not internal layers) in this Application Note, and therefore at most double-sided (2 layer) boards.

Using the thickness of the copper trace we can find the trace width required. For example for 1 oz copper board (1.4 mils copper thickness), and allowing 20˚C rise in temperature, for 4A of current we need 75/1.4=54 mils (1.4 mm) wide trace. For a 2 oz board we need exactly half of that i.e. 0.7 mm width.

However note that a 1 oz double sided board will pass through an electroless copper plating process stage (before solder mask is applied) to create the vias (/PTH: Plated Through Hole), and so it may end up effectively as being considered closer to a 1.4 oz copper board. Therefore it is a good idea to check this out with the PCB manufacturer before even starting the layout. Also note that even a single-sided board passes through a hot air solder level finishing stage (after solder mask), where a thin Tin-Lead layer is deposited on the 'unmasked' (no solder mask) copper areas. This does increase the effective thickness of these traces, but doesn't help as much as copper plating, since Tin-Lead has 10 times higher resistivity than copper.

When estimating resistive heating, it is important to know the average current in the traces. For a Buck converter, in the AC traces of the input sections (the left hand side of the IC in *Figure 1c*) the average current is Io*D, where Io is the load current and D the duty cycle. For the AC traces of the output section (the right-hand side), the average current is Io*(1-D). So if the load current is 3A, and the duty cycle (≈Vo/Vin) is say 0.4, then the average current on the input side is 1.2A only. On the output side it is 1.8A. In neither case is this equal to the load current of 3A! So the trace should be sized correctly and according to such a calculation.

Note that the expected temperature rise stated above is based on 'self-heating'. But a trace can become very hot simply due to heat from a nearby component. In that case, even a 30˚C (additional) rise due to self-heating may be unacceptable. And the 'acceptable' rise also depends on worst-case ambient temperature, and also the rated temperature of the board laminate (keep below 120˚C for FR4).

A quick thumb rule that closely follows the above discussion is:

For moderate temperature rise (less than 30˚C) and currents less than 5A

- Use at least 12 mils width of copper per amp for 1 oz board
- Use at least 7 mils width of copper per amp for 2 oz board

B) TRACE INDUCTANCE

We have seen that the preferred method to reduce trace inductance is to reduce length, not increase width. Beyond a certain point, widening of traces does not reduce inductance significantly. Nor does it depend much on whether we use 1 oz or 2 oz boards. Neither does it depend on whether the trace is unmasked or not (to allow solder/copper to deposit and thereby increase effective conductor thickness). But if for some reason the length cannot be reduced, another way to reduce inductance is by paralleling of forward and return current traces.

Inductances exist because they can store magnetic energy. Therefore conversely, **if the magnetic field is somehow cancelled, the inductance too vanishes**. By paralleling two current traces, each carrying current of the same magnitude but in opposite direction on a PCB, the magnetic field is greatly reduced. These two traces should be parallel and very close. They can be run side-by-side on the same side for a single-sided board. If a double-sided PCB is being used, the most effective solution is to run the traces parallel and on opposite sides of the PCB. The traces can and should be fairly wide in this case to improve their mutual coupling and create the required field cancellation. Note that **if a ground plane is used on one side, the return automatically 'images' the forward current trace and produces field cancellation and reduction in inductance**.

The designer may well ask: what happens to the inductance equation for trace length we presented earlier? ---that didn't seem to indicate that paralleling should help. The problem with the simple trace inductance equation is that it is an approximation. **There is simply no such thing as an independent straight piece of wire carrying current in a given direction --- current must return and so there are only current loops**. This follows from basic Physics --- charge cannot accumulate and must return: in this case to the opposite terminal of the emf source responsible for the flow of current. So whenever we talk about the inductance of just a single wire, basically we are talking about a very large loop. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance too is reduced.

Copper Filling: when to Stop

(Continued)

C) THERMAL MANAGEMENT

Natural convection depends on the amount of surface area that is in contact with the air. If a conductive plate serving as a 'heatsink' is thick enough to ensure perfect thermal conduction into the far recesses of the plate, the temperature rise would have been simply inversely proportional to the total exposed area. PCB copper planes too are in that sense an aid to convection, the difference being that they are not thick enough to ensure perfect conduction. Therefore at some point, we will reach a point of diminshing returns: very large increases in the copper area will produce smaller and smaller improvement in the thermal resistance. This occurs roughly for a square of side 1 inch on a 1 oz copper board. Some improvement continues till about 3 inches, especially for 2 oz boards and better, but beyond that, external heatsinks are required. Ultimately, a reasonable practical value attainable for the thermal resistance (from the case of the power device to the ambient) is about 30˚C/W.

That is not to say that heat is lost only from the copper side. The usual laminate (board material) used for SMT applications is epoxy-glass 'FR4' (also known as GF or G10) which is a fairly good conductor of heat. More commercial and cost-effective applications use cheaper board materials like CEM1, CEM2, CEM3 etc., which are fortunately not much worse as thermal conductors than FR4. So some of the heat from the device side does get to the other side where it contacts the air. Therefore **putting a copper plane on the other side (this need not even be electrically the same node, it could be the ground plane) also helps, but only by about 10%–20% as compared to a copper plane on only one side. A much greater reduction of thermal resistance by about 50%–70% can be produced if 'thermal vias' are used to conduct heat to the other side.** This thermally 'shunts' or bypasses the board material to get the heat to the other side where there is more exposure to air movement.

The tab of the power packages of the Simple Switcher devices is fortunately at Ground potential, so having large copper planes around the tab will not produce EMI. The tab can be left floating, but if it is used, it must be physically connected directly to the GND pin of the IC as indicated in *Figure 2*. If a double-sided board is used, several small vias can be sunk right next to the IC Ground in positions marked 'X' on to a 'Ground plane' on the other side of the PCB. These vias therefore not only help in the correct electrical implementation of grounding, but also can serve as thermal shunts. They are therefore appropriately called **'thermal vias'. It is recommended that they be small (0.3 mm–0.33 mm barrel diameter) so that the hole is essentially filled up during the plating process, thus aiding conduction to the other side. Too large a hole can cause 'solder wicking' problems during the reflow soldering process. The pitch (distance between the centers) of several such thermal vias in an area is typically 1 mm–1.2 mm and a grid of thermal vias can be created right under the tab.** Since the thermal vias also 'steal' heat away from the area during the reflow cycle, occasionally leading to poor solder joints, some recommend that vias (thermal or otherwise) should be close to, but never directly under the tab/legs/pins of any component.

From the point of view of the internal construction of a typical switcher IC, there is no reason to make the trace around the switching node wide since very little heat can come out this way. As mentioned earlier, this node can act as an antenna and cause radiation problems. However, there are situations where a large amount of copper on the switching node may just be unavoidable. The tab of most power diodes is the cathode. To sink heat from the diode, a large heatsink or copper plane must be connected to the tab. Unfortunately for a conventional positive to positive Buck topology (unlike the positive to positive Boost or the negative to positive Buck-Boost) the cathode/tab of the diode corresponds to the switching node, which is not 'quiet'. Therefore we have a conflict of interest here between thermal requirements and EMI. For EMI-sensitive applications, a rather non-typical diode with the anode internally connected to the tab can be sought. Or, if an external heatsink is being used, it is recommended that there be electrical (not thermal!) isolation between the power device and the (grounded) heatsink. Mica or 'Sil-pads' are possible choices here. If the diode must be SMT, an isolated SMT package may be a good choice.

Overestimating the amount of the copper plane for device cooling is a common mistake, and can lead to excessive EMI. **The heating in a Buck converter diode is based on the average current through the diode, not the load current.** Note that a typical Schottky diode has a forward voltage drop of 0.5V. If the load current is 5A and the duty cycle is 0.4, the dissipation is only 5*0.5*(1–0.4)=1.5W. If the temperature of the board (the copper area around the tab) is to be say a maximum of 100˚C, and the maximum ambient is 55˚C, the allowed temperature rise here is 100–55=45˚C. For 1.5W of estimated dissipation, the required board (or case) to ambient thermal resistance is 45/1.5=30˚C/W. This as we have seen is achievable on a PCB. To calculate the required area, **we can use as a good approximation an equation derived from empirical equations for a plate of area 'A'**:

$A = 985 \times Rth^{-1.43} \times P^{-0.28}$ sq.inches

Here P is in Watts and Rth is the required thermal resistance in ˚C/W. Solving for our example

$A = 985 \times 30^{-1.43} \times 1.5^{-0.28}$ sq.inches

A = 6.79 sq.inches

If this area is square in shape, the length of each side needs to be $6.79^{0.5}$ = 2.6 inches. **If the area called for exceeds 1 sq inch, a 2 oz board should be used.** Clearly a 2 oz board should be used in the example, as it reduces the thermal 'constriction' around the power device and allows the large copper area to be more effectively used for convection. Note that we are considering only a copper plane exposed to air on one side of the PCB. Breaking up the Ground plane to create islands on the other side to connect to was not considered a good option as it leads to odd return current patterns.

The Ground Plane

With double-sided boards, it is a common practice to almost completely fill one side with ground. There are people who usually rightly so consider this a panacea or 'silver bullet' for most problems. As we have seen, every signal has a return, and as its harmonics get higher, the return 'wants' to be directly under the signal path, thus leading to field cancellation, and reduction of inductance. It also helps thermal management as it couples some of the heat produced by power devices on one side of the board to the other side. The Ground plane also capacitively links to noisy traces above it, causing some 'softening' of transients and thereby some reduction in noise/EMI ---**unless the cross-coupling is so severe as to start causing the Ground plane itself to**

The Ground Plane (Continued)

radiate. Vias can be sunk under the ground terminal of all power components in to the Ground plane, and this reduces DC resistance offset errors on the output voltage too for example. As mentioned, in *Figure 2*, 'X' marks have been placed to indicate that if there is a double sided board in use, and a Ground plane is present, then vias can be added at these points. They are optional, and so if a low cost single-sided board is preferred, they can be omitted. But if these vias are also doubling over as 'thermal vias' for the switcher IC, as when they are under the tab of an SMT power device, they should be sized appropriately as previously discussed.

However, a Ground plane should be an 'add-on' to the recommendations in *Figure 2*. It does not substitute the correct placement of the two critical components. Much effort should go into not breaking or partitioning this plane. Further, in general, if too much switching power flow occurs through such a plane, it can create 'ground bounce' and cause controller upsets. Therefore in higher power applications, with the added luxury of multi-layer PCBs, separate signal and power ground planes are used. But for the lower power SIMPLE SWITCHER family, a single Ground plane is all that may be required. And if the layout is carried out conscientiously , keeping all the recommendations in mind, even a single-sided board should suffice.

Signal Traces: Feedback

The only critical signal trace is the feedback trace. First consider only the Adjustable versions of the Simple Switchers. One end of the trace connects to a low impedance node, which is the output rail or a resistive divider at the output. The other end connects to the feedback pin, which is the high impedance input of the error amplifier. If this trace picks up noise (capacitively or inductively) as it passes between these two nodes, it can lead to erroneous output voltages, and in extreme cases even instability or device failure. There seem to be just two options for this

1. Keep the feedback trace short if possible so as to minimize pickup AND/OR
2. Keep it away from noise sources (e.g. switching diode, inductor)

Keeping the trace short may not be feasible. In fact **the feedback trace may be deliberately kept slightly longer so as to route it away from potential noise sources.It should not pass under the inductor or diode in particular.** If a double-sided SMT board is being used, a good strategy is as follows:

- use a via at the output resistive divider to bring the trace to the other side
- run the trace to cut through the surrounding ground plane areas, taking care not to pass it under the inductor/diode and not parallel to any power trace on either side of the board (though it can cross them perpendicularly)
- and then very close to the IC, use another via to bring out the trace to the component side where it connects to the feedback pin of the IC

Refer to *Figure 5a* which shows the situation for the Adjustable part. The trace which picks up noise is bold. However, if we consider a fixed voltage part, we learn an important thing. This is *Figure 5b*. Note that the feedback trace here is not marked bold. The reason is that **a trace can pick up noise only if at least one end of it is a high impedance node**. In *Figure 5b*, the feedback pin goes to a resistive divider rather than directly to the input of the error amplifier. So it is relatively immune to noise pickup. The only section where noise can be picked up is inside the IC (shown bold), and this is a very short path. Applying the same principle to an Adjustable part provides another interesting way to route the feedback trace. One way is shown in *Figure 5c*. Here the length of the 'feedback trace' is very short, so it is relatively noise-free. The feedback resistors are physically close to the IC and the trace from the output to the upper resistor has low impedances on either side, and so does not pick up noise. However, the connection of the lower resistor to ground is not ideal as the resistive drop across the section marked 'Io*R' will affect the output voltage load regulation slightly. **Another way is in Figure 5d, and this resolves both issues. This is therefore recommended.** If a ground plane is used however, both *Figure 5c* and *Figure 5d* are actually the same if vias are correctly placed to couple into this plane. For *Figure 5d*, if possible, it is a good idea to run the top and bottom traces to the resistive divider parallel and close to each other, so as to minimize any further chance of noise pickup.

Signal Traces: Feedback (Continued)

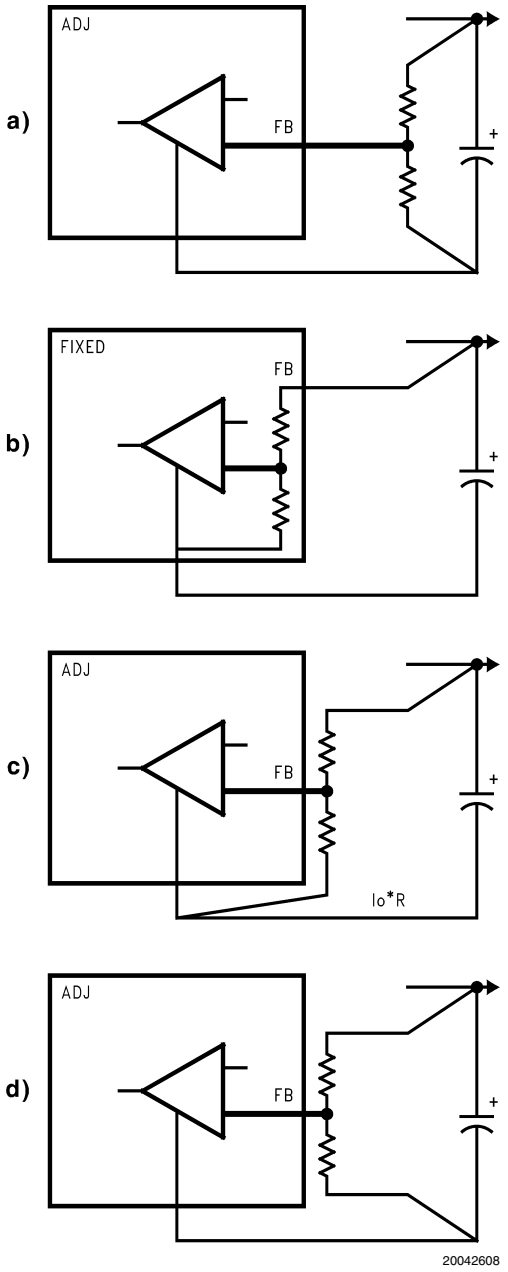

FIGURE 5. Feedback Traces (bold lines susceptible to noise)

Notes

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National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507